Simulation and Analysis of Gate Current Through Hf-based High-k Structures for nanoscale MOSFETs

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Abstract

We use a quantum-mechanical model to study the gate tunneling current of Hf-based high-k dielectric films for nanoscale MOSFETs. The three-dimensional gate current component evaluation is performed by the traveling wave calculations for the thermionic emission, Fowler-Nordheim (FN) tunneling, and direct tunneling through the oxide barrier. For the two-dimensional gate current component originated from the subbands in the inversion layers, a transmission calculation is performed. Various Hf-based high-k structures and materials of interest have been examined and compared to access the reduction of gate current in these structures. Effects of nitrogen content, hafnium content, aluminum content, and interfacial layer (IL) on the gate tunneling current have been studied theoretically. Our results show that the reduction of the gate tunneling current can be optimized in terms of the nitrogen content, aluminum content, and the composition of the IL. Our computational results are in very good agreement with experimental data.

Keywords: *High-k；Gate current；Quantum-mechanical model*

1. Introduction

With the scaling down of the MOSFETs into the sub-100 nm regime, high-k materials are being introduced to achieve a greater physical thickness of the dielectric layer and reduce the gate tunneling current while retaining an equivalent oxide thickness and performance. Among all the high-k materials being considered, HfO_2 is one of the promising candidates for use as the gate insulator due to its wide bandgap (~5.8 eV) with band offsets of 1.5 eV to silicon, high dielectric constant and compatibility with conventional complementary metal-oxide-semiconductor (CMOS) process. However, HfO_2 exhibits a low crystallization temperature(~375℃) [1]，which leads to the formation of grain boundaries, resulting in higher leakage current and severe boron penetration which degrades device performance. More recently, incorporation of Al, Si ,Ti, Ta and N elements into HfO_2 has been proposed to alleviate the problem. The hafnium-based dielectric films, such as $(HfO_2)_x(SiO_2)_{1-x}$ or HfSiO, N-incorporated HfSiO or HfSiON, $(HfO_2)_x(Al_2O_3)_{1-x}$ or HfAlO, and HfTaTiO are being actively investigated and reported to show better thermal stability, increased crystallization temperature and improved carrier mobility as compared to HfO_2 [1-6]. However, although numerous experimental studies have been conducted, few theoretical efforts have been devoted to studying effects of the element incorporation on the gate tunneling current for these device structures [7, 8].

In this paper, physical modeling of tunneling currents through Hf-based dielectric films based on a self-consistent solution to the Schrödinger and Poisson equations is presented. Although a couple of modeling research work has been reported for tunneling current through HfO_2 and HfO_2 alloys[7,

[8], they were based on empirical or WKB modeling approaches where aspects of device physics are parameterized and fitting parameters must be used to reach agreement with experiment. In the present approach, only adjustable parameter is the electron effective mass when it is not available accurately.

2. Modeling

In previous studies, an accurate model[9-11] based on self-consistent solution of the Schrödinger-Poisson equations have been successfully developed for modeling quantum tunneling devices, such as the resonant tunneling diodes and transistors. In this work, the modifications are made for nanoscale MOSFETs in the y direction perpendicular to the dielectric layers as shown in
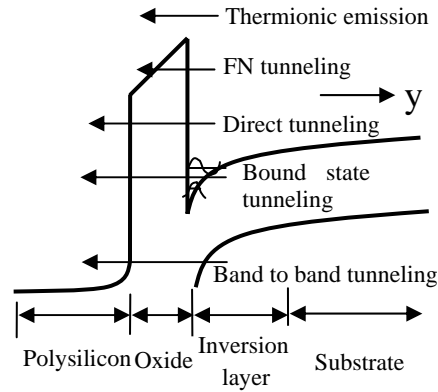

Fig. 1 Schematic gate current components in
nanoscale MOS structure

Fig. 1. The gate current components of the thermionic emission, FN tunneling , direct tunneling and band to band tunneling through the oxide barrier are evaluated as a whole using a traveling wave calculation, hereafter referred to as J_{3D}, while the tunneling component from the inversion layer quantum well is evaluated by a transmission calculation, hereafter referred to as J_{2D}, both obtained from the solutions of the Schrödinger equation, self-consistently with its potential term determined by the Poisson equation. We first calculate the self-consistent potential and charge distributions in the polysilicon and substrate regions from the coupled Poisson equation and Fermi distribution function. The Poisson equation and the Fermi integral lead to a pair of coupled nonlinear equations[9,10], which are then solved using the Newton iterative method with a sparse matrix technique.

For the charges inside the inversion layer quantum well formed under positive gate bias voltages, and for the gate current components through and/or above the ultrathin oxide barrier, quantum calculations are performed by directly solving the Schrödinger equation.

$$-\frac{\hbar^2}{2}\frac{\partial}{\partial y}\left(\frac{1}{m^*(y)}\frac{\partial \psi(y)}{\partial y}\right)+E_C(y)\psi(y)=E\psi(y) \tag{1}$$

The self-consistent electron density at the *j*th energy subband in the *i*th valley in the inversion layer is given by

$$n_{ij}(y) = \frac{m_i^* k_B T}{\pi \hbar^2} \ln\left[1 + \exp\left(-\frac{E_{ij} - E_F}{k_B T}\right)\right] \times \left|\psi_{ij}(E_{ij}, y)\right|^2 \tag{2}$$

where $\psi_{ij}(E_{ij}, y)$ is the electron wavefunction at the *j*th subband in the *i*th valley from the solution of the Schrödinger equation in the inversion layer. The gate current evaluation is performed by the traveling wave calculations for the thermionic emission, FN tunneling, and direct tunneling through the oxide barrier, giving[9]

$$J_{3D} = -q\hbar \sum_k W(k) \operatorname{Im}\left(\psi_k^*(y) \frac{1}{m^*(y)} \frac{\partial \psi_k(y)}{\partial y}\right) \tag{3}$$

where $W(k)$ is weighting function of the source electrons in the electrodes[9]. For the electron tunneling current from the inversion layer into the oxide and gate electrode, a transmission calculation is performed[10]. Based on the wave functions calculated in the inversion layer, the transmission is given by[10]

$$T_{ij} = \frac{\left|C_{tr,ij}\right|^2}{\left|A_{in,ij}\right|^2} \frac{k_{tr,ij}}{k_{in,ij}} \frac{m_{in,i}^*}{m_{tr,i}^*} \tag{4}$$

where $C_{tr,ij}$ is the transmitted wave amplitude in the *i*th valley and the *j*th subband, and $A_{in,ij}$ the incident wave amplitude in the corresponding subband and valley, respectively. The 2D gate current component originated from the subbands in the inversion layers is then

$$J_{2D} = \sum_{i,j} J_{i,j} = q \sum_{i,j} n_{e,ij} T_{ij} f_{ij} \tag{5}$$

where T_{ij} is the electron transmission probability, $f_{ij} = \dfrac{E_{ij}}{j\pi\hbar}$ the interface impact frequency, $n_{e,ij}$ the sheet electron density, and E_{ij} the quasi-bound state energies, in the *i*th valley and the *j*th subband, respectively. The total gate current density is the sum of the 2D and 3D components.

In the present approach, we treat the thermionic emission, FN tunneling, and direct tunneling current components in a unified formulation. Note that in our modeling calculations, the electrostatic potential *V(y)* and the material parameters can be specified at each point in the multilayered stack structures, allowing evaulation of various schemes of combination having different stack materials and different layers. In addition, the possible fixed charge and interface

charge distributions in the stacked layers can also accommodated in Possions' equation, as long as models for these charge distributions are available. Therefore, the present approach is very suitable for study of multilayer high-k stack structures of nanoscale MOSFETs. More details of the method of calculation are described in[9-11].

3 Results and discussion

3.1 Gate tunneling current through HfSiO and HfAlO

It has been reported that hafnium silicate (HfSiO) has a better thermal stability on silicon substrates than HfO_2[2]; it provides a relatively high dielectric constant (5~25) and a wide band-gap (6~11eV) as compared to that of SiO_2[12]. It is reported that increasing Si composition in HfSiO layer produces a higher drive current. However, this improvement was achieved at the expense of a higher gate leakage current [12].
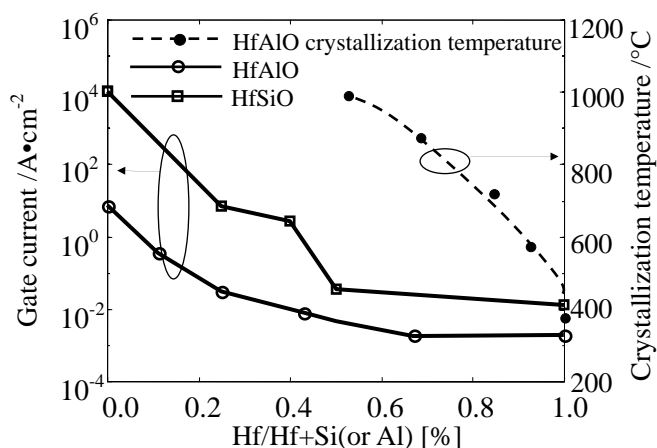

Fig. 2 Crystallization temperature of HfAlO and simulated tunneling currents through HfAlO and HfSiO dielectric films as functions of hafnium content. Data of crystallization temperature are from [1]. For HfAlO, the dielectric constants of HfAlO are from [1], the conduction band offset values of HfAlO are from [13], and the electron effective masses are linearly interpolated from that of HfO_2 (m= $0.1m_0$ [14]) and $Al_2 O_3$(m= $0.35m_0$ [15]). For HfSiO, the dielectric constants are from [12], the conduction band offset values are from [6], and the electron effective masses are linearly interpolated from that of HfO_2 and SiO_2(m= $0.5m_0$ [16])

Al inclusion in HfO_2, which forms HfAlO, increases the crystallization temperature even above ~1000℃ [2]. It was found that the higher the Al content, the higher the crystallization temperature of the HfAlO (see Fig.2). This is probably because the Al acts as a network modifier and stabilizes the amorphous phase of the metal oxides [1]. Adding Al into the HfO_2 results in an increase of the band gap and a decrease of dielectric constant as compared to HfO_2. HfAlO is more thermally stable than HfSiO. Therefore, HfAlO seems to be a more suitable material than HfSiO.

In Fig.2, the calculations are for the study of effects of hafnium content on the gate current for

HfAlO and HfSiO dielectric films, using the same V_g=0.8V and the EOT of 0.9nm. We have the following observations from the results shown in Fig. 2: (1) The general trend of decreasing gate current with increasing hafnium content; (2) It is seen that more Al or Si incorporation, although having the advantage to suppress the increase the crystallization temperature and bandgap, will lead to an overall increase of the gate current due to the decrease of the dielectric constant. (3) It is found from our calculations that an optimum value of the Al content of between 0.3 to 0.4 would be desirable to gain the advantage of Al incorporation while still avoid significant increase of the gate current. This is consistent to the results of previous studies of the influence of the Al content on the gate current [7, 8], for that the interplay between the crystallization temperature and dielectric constant reaches an approximate optimum value of the Al percentage ,which can raise the HfAlO crystalline temperature above 900°C; (4) For the same Hf content, the gate current density for the HfSiO is larger than that for the HfAlO due to the lower dielectric constants[10].

3.2 Gate tunneling current through HfSiON

It is known that the use of HfSiO with low Si composition is insufficient to produce a low leakage current while having a high driving current for use in high performance or low power devices[12]. Incorporation of nitrogen to form hafnium silicon oxynitride (HfSiON) increases the dielectric
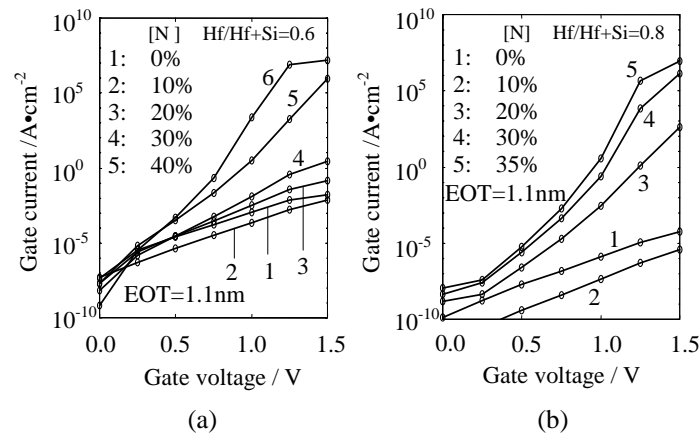

Fig. 3　Tunneling current through HfSiON dielectric films for different N contents. The EOT is 1.1 nm for all the calculations and the electron effective mass is taken to be 0.27m_0. The dielectric constant and electron barrier height of HfSiON are taken from [6].(a) Hf/(Hf+Si)=0.6; (b) Hf/(Hf+Si)=0.8

constant of silicates because the nitrogen atoms in HfSiON probably enhance the electronic polarization as well as the ionic polarization. Incorporation of nitrogen also suppresses boron penetration through the film during high temperature annealing due to Si-N bonds being more robust to resist interface states generation [17,18]. It is reported that this material has superior electrical characteristics such as low interfacial trap density and scalability to equivalent oxide thickness of less than 10 Å. This material also has the advantage of being thermally stable up to 1100 °C in contact with poly Si [19].

In Fig. 3, the effects of N composition on the gate current are shown for tunneling current through

HfSiON dielectric film. Three different electron effective masses in between that of SiO_2, HfO_2, and Si_3N_4 were used in the calculations as the value of the electron effective mass is not available, and such modeling calculations have not been found in the open literature. However, the values of dielectric constant and barrier height were taken from experimental work with the N content up to 50% in the Fig.3(a), and up to 35% in the Fig.3(b) [6]. The results here show that, for both cases, there is an optimum value of the N content (approximately 10 %) where minimum gate current may be achieved and the optimized HfSiON can reduce the leakage current by above two orders of magnitude at Vg=0.5~1.0V. This is attributed to the interplay between the dielectric constant and barrier height; the incorporation of N leads to an increase of the dielectric constant while maintaining essentially the same barrier height until the N content reaches 10% where the barrier height start decreasing significantly[6]. This optimum value of N content is a new finding to be verified experimentally.

3.3 Gate tunneling current through HfTaTiO

The reported dielectric constants of HfSiON and HfAlO are below 26, which limits the further scaling to sub-nanometer regime where the gate leakage becomes a critical issue. HfTaTiO dielectrics are considered to be prospective high-k materials due to their very high permittivity
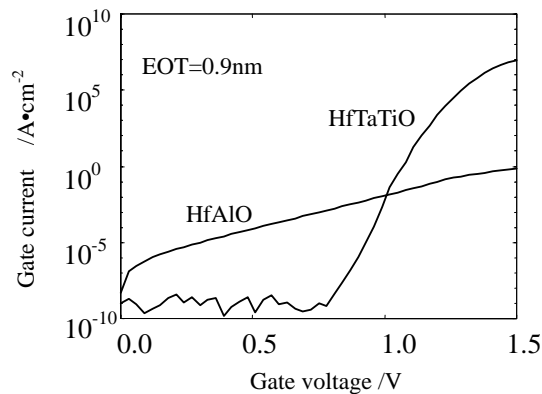

Fig. 4 Tunneling current through HfTaTiO and HfAlO films. The material parameters of HfAlO (Hf/(Hf+Al)=0.35) are as same as that in Fig.3. The dielectric constant, electron barrier height and electron effective mass of HfTaTiO are 56.0,1.0eV and 0.25 m_0 [20], respectively.

(~60) , high electron mobility, acceptable barrier height relative to the Si conduction band (~1.0 eV) , and high crystallization temperature (~ 900 °C)[20-21]. The increase of dielectric constant in thin laminated layer structures could be ascribed to the improvement of molar polarizability. When a robust Ti–O–Hf network is formed, resulting in an amorphous and homogenous film, incorporation of highly polarizable cation Ta^{5+} increases its the dielectric constant and crystallization temperature[20].

Fig. 4 shows gate current vs. gate bias voltage for HfAlO and HfTaTiO gate insulators, using the

same EOT of 0.9nm. The optimized material parameters of HfAlO（[Al]=35%）are used. It is observed that the gate current for HfTaTiO film is about five orders of magnitude less than that of HfAiO film at low biases, due to the thicker physical width in the tunneling path for the lower energy electrons that contribute most of the gate current. However, as the gate voltages go higher, the reduction of gate current is ineffective somewhere near and above the barrier height of the high-k dielectric layer, due to the dominating FN tunneling and thermal emission near and over the barrier of the high-k layer, although this is not a serious concern for the bias range of nanoscale MOS devices. In other words, the high dielectric constant of HfTaTiO has played a major role for the reduction of gate current, although it is recognized that the high dielectric constant has to be coupled with a high barrier height to suppress the gate tunneling effectively, while at higher bias, it is mainly determined by its barrier height. In addition, at low gate voltages, oscillations and kinks may occur in the calculated curves especially for thicker high-k layers. This is believed to be caused by pronounced multiple quantum reflections inherent in this type of quantum calculations in which the integration of wave functions may approach numerical instability. This type of oscillation has also been observed in other published works [22,23].

As a result of the above-mentioned advantages of HfTaTiO dielectrics, we believe that, with supply-voltage scaling, HfTaTiO is the most probable candidate for long-term solutions as alternative high-k gate dielectrics.
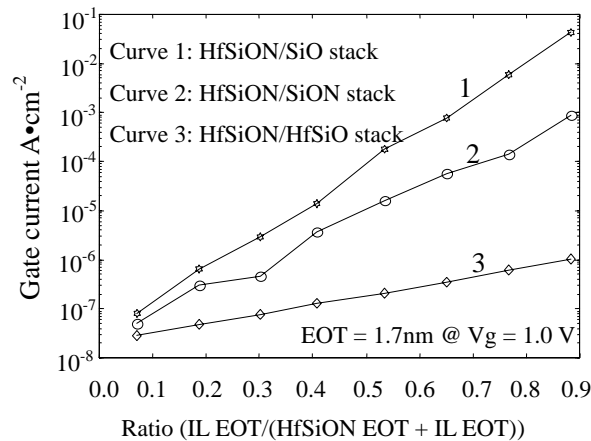
3.4 Effects of Interfacial layer (IL)

Fig. 5　The ratio dependence of IL on tunneling current through HfSiON stack. The percentage of Hf/(Hf+Si) for HfSiON is 60%. The N content of HfSiON is 10%. The electron barrier height, dielectric constant, and electron effective mass of SiON is taken from [24].

In practical applications , an ultrathin interfacial layer, which generally forms during the fabrication process, has been used to improve the interface quality and the channel mobility. In Fig. 5, the interfacial layer effects are examined for structures of HfSiON/SiO$_2$, HfSiON/SiON, and HfSiON/HfSiO, with the corresponding curves 1, 2 and 3, respectively. The ratio dependence of IL on gate tunneling current through HfSiON stack dielectric films with an EOT of 1.7nm. The horizontal axis is the ratio of the EOT of the IL to the total EOT of the film including the IL. It is apparent that the tunneling leakage current increases significantly with the increase of thickness of

IL which have lower dielectric constants, and that among the three kinds of IL studied, the HfSiON/HfSiO structure gives the lowest possible gate current due to its relatively higher dielectric constant. The influence of the lower-k IL is seen to be significant unwanted for the high-k dielectric stack structures from the gate leakage current viewpoint, although the ultra-thin lower-k IL improves the interface quality and threshold voltage roll-off. Therefore, control of the interfacial layer thickness and optimization of the stacked ratio is very important to future scaling of the gate dielectric.
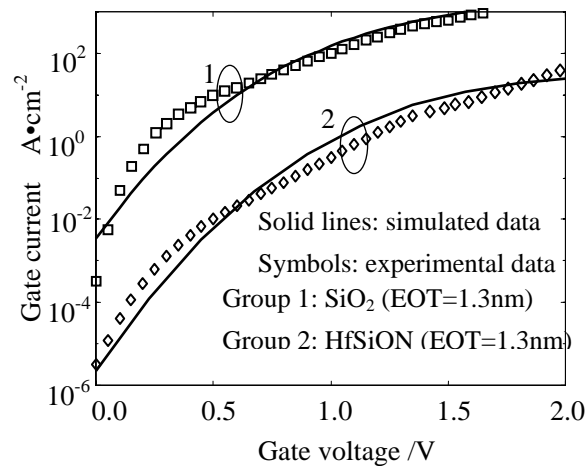
3.5 Comparison with experimental

Fig. 6 Comparison with experiment. The symbols are experimental data taken from [7, 25]. The dielectric constant of HfSiON is 7.0 taken from [25], the electron barrier height is 2.86 eV taken from [26], and the electron effective mass is taken to be $0.27m_0$.

Then our modeling results are compared with available experimental data. Fig. 6 shows gate current dependence vs. gate bias voltage with different material parameters. The group curves 1, 2 correspond to SiO_2 (EOT=1.3nm) and HfSiON (EOT=1.3nm), respectively. The symbols of 1 and 2 are experimental data taken from [25]. Very good agreement has been achieved between our modeling results and the experiment data. However, the measured gate current is somewhat larger than the simulated values at the low bias voltages. This is probably contributed by tunneling current components between the source and drain, and via interface states.

High-k stack dielectric structures have received great attention in the past several years due to their practical significance in microelectronics industry. Numerous studies of high-k structures have been conducted. The research results so far published have shown promising future. However, due to uncertainty in material parameters, such as barrier height, dielectric constant, electron effective mass, which are difficult to be determined accurately for new dielectric stacks, published modeling and experimental results show some inconsistency. As the present modeling approach enables us to specify material parameters in the individual regions of combinations of high-k materials and structures, a greater variety of these combinations can be studied using this approach.

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The modeling calculations for the HfSiO(N) and HfTaTiO structures reported in this paper are believed to be the first modeling attempt for these structures.

4   Summary

A numerical model based on solutions to the Schrödinger-Poisson equations is utilized to study gate tunneling current of Hf-based dielectric films for nanoscale MOSFETs. In particular, effects of nitrogen content, hafnium content, and interfacial layer (IL) on the gate tunneling current have been studied. The results obtained in this study show that the reduction of the gate tunneling current can be optimized in terms of the nitrogen content, the aluminum content, and composition of the interfacial layer. Our computational results are in very good agreement with experimental data. This approach may be used to provide a design aid for nanoscale MOSFETs.

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